EXHIBIT 5

Case 2:21-cv-00463-JRG-RSP Document 73-9 Filed 06/26/22 Page 2 of 98 PageID #: 3012

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC, Plaintiff, vs. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., Defendants.	))))))))))))	Civil Action No. 2:21-CV-463-JRG JURY TRIAL DEMANDED [redacted]

EX. A TO 4-3 JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT (DKT. 70)

EXHIBIT A

[redacted]

Claim Construction Positions and Supporting Evidence[1]

I. Proposed Constructions

a. U.S. Patent Nos. 11,016,918 and 11,232,054

Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
'918: 1-3, 5-7, 9-13, 15, 21	"a second plurality of address and control signals"	Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, a second set of address and control signals).	'918, claim 1 ("at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices"). '918, 21:65-22:34 ("The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown). For example, the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and	[redacted] Petition in IPR2022-00996, at 23:

[1] NB: Other than citations to dictionaries, the citations referenced are examples only. The entire document is relevant.

[2] [redacted].

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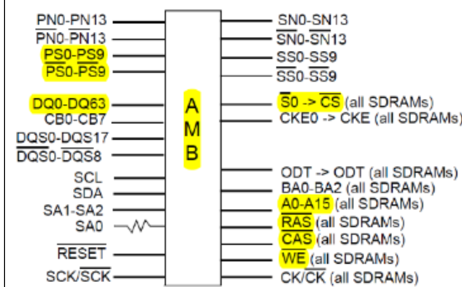
Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector. [¶] The volatile memory subsystem 1030 comprises a plurality of volatile memory elements 1032 and the non-volatile memory subsystem 1040 comprises a plurality of non-volatile memory elements 1042. … In certain embodiments, the first plurality of volatile memory elements 1032 comprises two or more dynamic random-access memory (DRAM) elements. Types of DRAM elements 1032 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and synchronous DRAM (SDRAM). For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises eight 64M×8 DDR2 SDRAM elements 1032. … In addition, volatile memory elements 1032 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. …."). 23:28-40 ("In certain embodiments, the at least one circuit 1052 comprises one or more switches coupled to the volatile memory subsystem 1030, to the controller 1062, and to the host computer (e.g., via the interface 1022, as schematically illustrated by FIGS. 12-14). The one or more switches are	 [redacted] Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify that in the context of the '918 and '054 patents, "a second plurality of address and control signals" means "a second set of address and control signals." In addition, if the expert disagrees with any of

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			responsive to signals (e.g., from the controller 1062) to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030 and to selectively operatively couple the controller 1062 to the volatile memory subsystem 1030. In addition, in certain embodiments, the at least one circuit 1052 selectively operatively couples and decouples the volatile memory subsystem 1030 and the host system."); *see also* 23:41-24:8. 5:33-36 ("Also described herein is a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols."); *see also*, 13:29-43, 16:56-17:13.	Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement.

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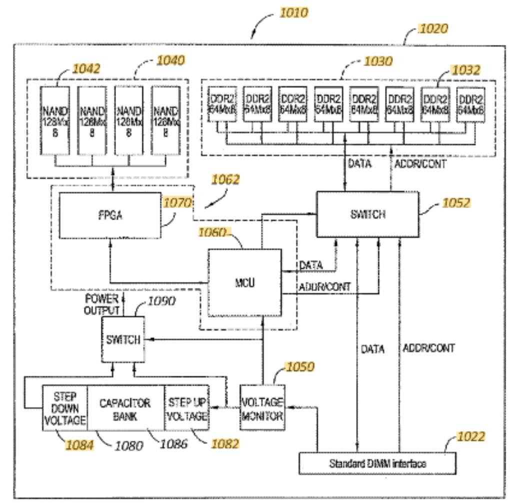
<table>
<tr><td></td><td></td><td></td><td>Figs. 12-14, 15A-15C:


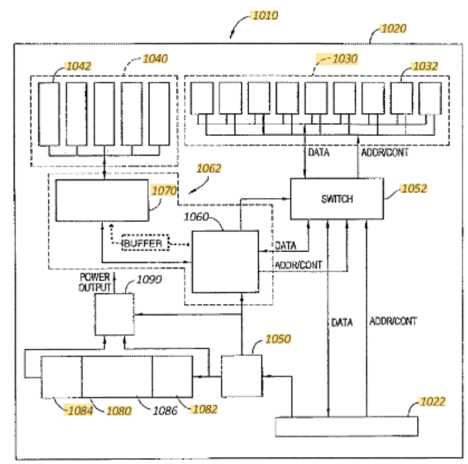
FIG. 12


FIG. 13</td><td></td></tr>
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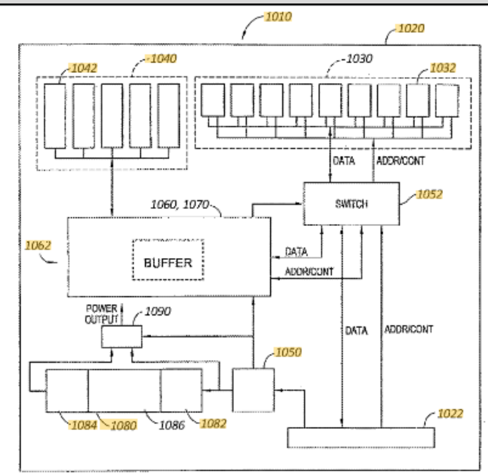
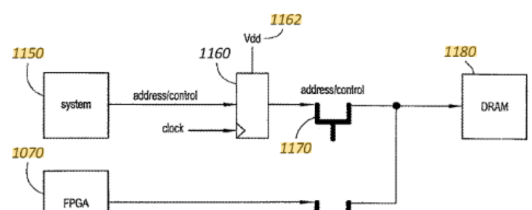
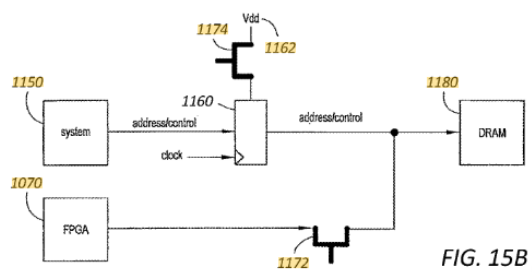
Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			 FIG. 14  FIG. 15A  FIG. 15B	

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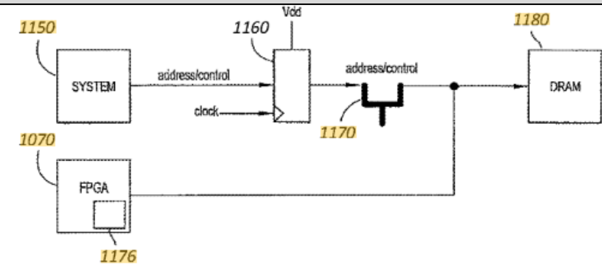
Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			 FIG. 15C	
'918: 2, 17, 28 '054: 15	"dual buck converter" / "dual-buck converter"	Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, a buck converter with two regulated voltage outputs whose amplitude may be the same or different).	29:18-31 ("The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub-blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16.").	Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify that in the context of the '918 and '054 patents, a "dual buck converter" means "a buck converter with two regulated voltage output whose amplitude may be the same or different." In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement.

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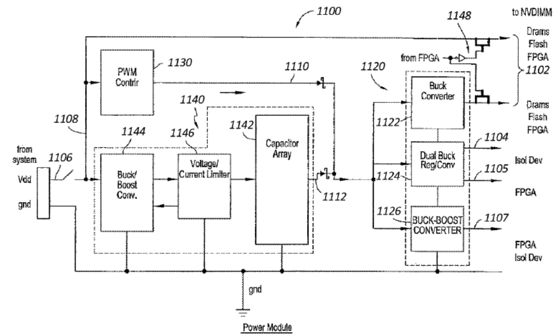
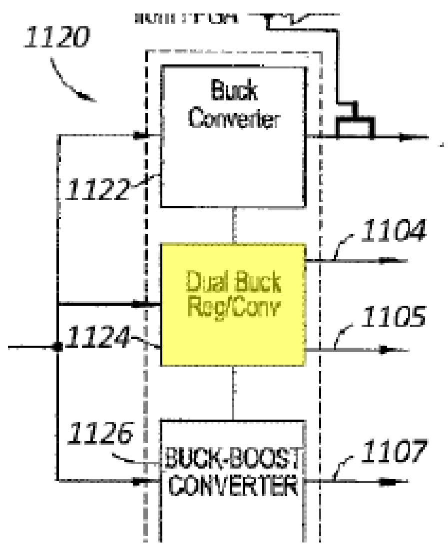
Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			Fig. 16  FIG. 16  	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
'918: 16-22, 30	"[pre-regulated] input voltage"	Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, voltage that is provided to the earlier mentioned converters or converter circuit).	'918, claim 16 ("first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively; a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage, wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively"). '918, 28:2-58 ("The power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems 1030, 1040. The plurality of voltages comprises at least a first voltage 1102 and a second voltage 1104. The power module 1100 comprises an input 1106 providing a third voltage 1108 to the power module 1100 and a voltage conversion element 1120 configured to provide the second voltage 1104 to the memory system 1010. The power module 1100 further comprises a first power element 1130 configured to selectively provide a fourth voltage 1110 to the conversion element 1120. In certain embodiments, the first power element 1130 comprises a pulse-width modulation power controller. For example, in one example embodiment, the first power element 1130 is configured to receive a 1.8V	Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify that in the context of the '918, claim 16, a [pre-regulated] "input voltage" means a "voltage that is provided to the earlier mentioned converters and converter circuit." In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			input system voltage as the third voltage 1108 and to output a modulated 5V output as the fourth voltage 1110. [¶] The power module 1100 further comprises a second power element 1140 can be configured to selectively provide a fifth voltage 1112 to the conversion element 1120. The power module 1100 can be configured to selectively provide the first voltage 1102 to the memory system 1010 either from the conversion element 1120 or from the input 1106. [¶] The power module 1100 can be configured to be operated in at least three states in certain embodiments. In a first state, the first voltage 1102 is provided to the memory system 1010 from the input 1106 and the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130. In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120. In the third state, the fifth voltage 1112 is provided to the conversion element 1120 from the second power element 1140 and the first voltage 1104 is provided to the memory system 1010 from the conversion element 1120. [¶]. In certain embodiments, the power module 1100 transitions from the first state to the second state upon detecting that a trigger condition is likely to occur and transitions from the second state to the third	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			state upon detecting that the trigger condition has occurred. For example, the power module 1100 may transition to the second state when it detects that a power failure is about to occur and transitions to the third state when it detects that the power failure has occurred. In certain embodiments, providing the first voltage 1102 in the second state from the first power element 1130 rather than from the input 1106 allows a smoother transition from the first state to the third state. For example, in certain embodiments, providing the first voltage 1102 from the first power element 1130 has capacitive and other smoothing effects. In addition, switching the point of power transition to be between the conversion element 1120 and the first and second power elements 1130, 1140 (e.g., the sources of the pre-regulated fourth voltage 1110 in the second state and the pre-regulated fifth voltage 1112 in the third state) can smooth out potential voltage spikes.”). Abstract (“In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage."). Figures 12-14, 15A-C and 16; Fig. 17 ("Provide first voltage from input power supply and second voltage from first power subsystem").	
'918: 16-22, 30	"pre-regulated input voltage"	Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, modulated input voltage).	*See* above.	Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify that in the context of the '918 claim 16, a "pre-regulated input voltage" means a "modulated input voltage." In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
				Webster's New World College Dictionary (4th Ed., 2000), at 1207 (regulate: "1 to control, direct, or govern according to a rule, principle, or system. 2. To adjust to a particular standard, rate, degree, amount, etc. *[regulate* the heat*]* 3 to adjust (a clock, etc.) so as to make operate accurately"), *id.* (regulator: "a person or thing that regulates; specif., *a)* a mechanism for controlling or governing the movement of machinery, the flow of liquids, gases, electricity, steam, etc.…"). Wiley Electrical and Electronics Engineering Dictionary (2004), at 649 ("3. To maintain a voltage, current, or the like, within specified values.").
'918: All asserted claims	"first" / "second" / "third" / "fourth" "regulated voltages"	Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, first, second, third and	Abstract ("In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third	Webster's New World College Dictionary (4th Ed., 2000), at 1207 (regulate: "1 to control, direct, or govern according to a rule, principle, or system 2. To adjust to a particular standard, rate, degree, amount, etc. *[regulate* the

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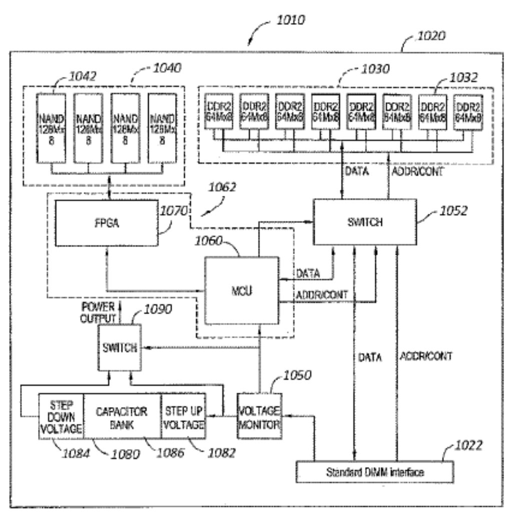
		fourth voltages that are adjusted, within tolerance, to a particular voltage level).	regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage.”)  26:36-43 (“When operating in the first state, in certain embodiments, the step-up	heat*]* 3 to adjust (a clock, etc.) so as to make operate accurately”), *id.* (regulator: “a person or thing that regulates; specif., *a)* a mechanism for controlling or governing the movement of machinery, the flow of liquids, gases, electricity, steam, etc.…”); *id.* at 1602 (voltage: “electromotive force, or difference in electrical potential, measured in voltages and equal to the current times the resistance”) Wiley Electrical and Electronics Engineering Dictionary (2004), at 649 (“3. To maintain a voltage, current, or the like, within specified values.”). Electronics: Definitions for the Digital Age (3rd Ed. 2007), at 350 (regulated voltage: “a voltage that remains steady, unaffected by changes in LOAD current or mains supply voltage”) Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			transformer 1082 keeps the capacitor bank 1086 charged at a peak value. In certain embodiments, the stepdown transformer 1084 acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (e.g., 1.8V to the volatile DRAM elements 1032 and 3.0V to the non-volatile flash memory elements 1042) when operating in the second state (e.g., during power down).") 29:18-54 ("The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub-blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various	light of the intrinsic evidence and knowledge of the person. The expert will testify that in the context of the '918 patent, a person of ordinary skill in the art would understand "regulated voltages" to mean voltages that are regulated, that is, voltages that are adjusted, within tolerance, to a particular voltage level (or amplitude). The expert will testify that in the context of the '918 patent, a person of ordinary skill in the art would understand first, second, third and fourth voltages need not all have different voltage levels (that is, they may all be different, some of the voltages may be the same, or all are the same), subject to other requirements of the claims. In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate amount for powering various components of the memory system. For example, the buck-converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The sub-block 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller	

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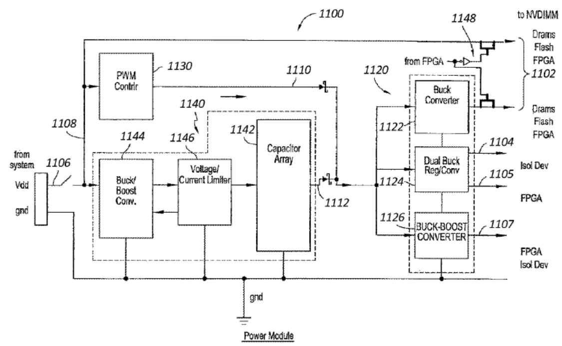
Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			1062 and the at least one circuit 1052.”).  FIG. 16	
’918: All asserted claims	“first” / “second” / “third” / “fourth” “voltage amplitude”	Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, first/ second/third/fourth amplitude of voltage which need not all be different).	*See* above.	Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify that in the context of the ’918 patent, a person of ordinary skill in the art would understand “voltage amplitude” to mean amplitude of a voltage. The expert will testify that in the context of the ’918 patent, a person of ordinary skill in the art would understand first, second, third and fourth voltage amplitudes need not all be

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
				different (that is, they may all be different, some of the voltage amplitudes may be the same, or all four amplitudes are the same), subject to other requirements of the claims. In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement.
'054: claims 1-15	"at least three regulated voltages"	Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, three or more regulated voltages).	*See* citations for '918 "regulated voltages."	*See* above for "regulated voltages" and "voltage amplitude."
'054: claims 16, 24 and dependent claims	"plurality of regulated voltages"	Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, multiple regulated voltages).	*See* citations for '918 "regulated voltages"	*See* above for "regulated voltages" and "voltage amplitude."
'054: 4-7, 11-12, 16-	"operable state"	Plain and ordinary meaning to a person	claims 4-7, 11-12 and 23 ("wherein the memory module transitions from a first	Expert testimony on the understanding by a person of

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
17, 23, 25-26		of ordinary skill in the art in light of the specification (that is, state in which the memory module is operated). For avoidance of doubt: "first operable state": "state in which the memory module is operated before transition"[3] "second operable state": "state in which the memory module is operated after transition"	operable state to a second operable state in response to the trigger signal"); claims 16-17, 25-26 ("wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state"); '918, 20:43-57 ("In certain embodiments described herein, the memory system includes a power module which provides power to the various components of the memory system from different sources based on a state of the memory system in relation to a trigger condition (e.g., a power failure). The power module may switch the source of the power to the various components in order to efficiently provide power in the event of the power failure. For example, when no power failure is detected, the power module may provide power to certain components, such as the volatile memory, from system power while	ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify that in the context of the '054 patent, a person of ordinary skill in the art would understand "operable state" means state in which the memory module is operated, such as a normal operating state, a state in which power failure was about to occur, a state in which power failure occurred and the like. In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement.

[3] Netlist disagrees that "operable state" refers to a "current" state of the memory module. Rather the "first operable state" refers to the state that the memory module is in before transition, that is, in the context of claims 4-7, 11-12 and 23, "state in which the memory module is operated when the trigger signal is produced" and in the context of claims 16-17 and 25-28, "state in which the memory module is operated when an amplitude change in the input voltage is detected." In contrast, the "second operable state" is the state that the memory module is in after transition.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			charging a secondary power source (e.g., a capacitor array). In the event of a power failure or other trigger condition, the power module may power the volatile memory elements using the previously charged secondary power source."); '918, 24:60-25:7 ("The memory system 1010 of certain embodiments is configured to be operated in at least two states. The at least two states can comprise a first state in which the controller 1062 and the non-volatile memory subsystem 1040 are operatively decoupled (e.g., isolated) from the volatile memory subsystem 1030 by the at least one circuit 1052 and a second state in which the volatile memory subsystem 1030 is operatively coupled to the controller 1062 to allow data to be communicated between the volatile memory subsystem 1030 and the nonvolatile memory subsystem 1040 via the controller 1062. The memory system 1010 may transition from the first state to the second state in response to a trigger condition, such as when the memory system 1010 detects that there is a power interruption (e.g., power failure or reduction) or a system hang-up."); *see also* 25:8-27:13.	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			28:39-58 ("In certain embodiments, the power module 1100 transitions from the first state to the second state upon detecting that a trigger condition is likely to occur and transitions from the second state to the third state upon detecting that the trigger condition has occurred. For example, the power module 1100 may transition to the second state when it detects that a power failure is about to occur and transitions to the third state when it detects that the power failure has occurred. …."); *see also* 28:26-38, 30:50-64.	
All asserted claims	"A memory module"	preamble is limiting	*See* '918, 3:66-7:67 ("Overview"), 9:66-10:1 ("Example embodiments are described herein in the context of a system of computers, servers, controllers, **memory modules**, hard disk drives and software."). *See also*, '918, FIGs. 3A-B, 4A-B, 5A-B, 7, 8A-B, 9, 13, 14, 15A-C, and accompanying description at 11:11-21, 11:41-12:2, 12:26-29, 12:52-13:25, 22:52-23:27, 23:41-44. *See also, e.g.*, 21:24-55 ("In certain embodiments, the memory system 1010 comprises a memory module. The memory system 1010 may comprise a printed-circuit board (PCB) 1020. In certain embodiments, the memory system 1010 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, or	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			8-GB. Other volatile memory capacities are also compatible with certain embodiments described herein. In certain embodiments, the memory system 10 has a non-volatile memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or 32-GB. Other non-volatile memory capacities are also compatible with certain embodiments described herein. In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the PCB 1020 has an industry-standard form factor. For example, the PCB 1020 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 1020 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 1020 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), miniDIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			embodiments described herein. For example, in other embodiments, certain non-DIMM form factors are possible such as, for example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI)."). *See also*, *e.g.*, '918 12:64-13:25 ("In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory subsystem which may be integrated with other components of a host system. In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory module that has the DIMM (dual-inline memory module) form factor, and may be referred to as a FDHDIMM, although it is to be understood that in both structure and operation it may be different from the FDHDIMM discussed above and described with reference to FIGS. 4A and 4B. Memory module 500 includes two on-module intermediary components: a controller and a data manager. These on-module intermediary components may be physically separate components, circuits, or modules, or they may be integrated onto a single integrated circuit or device, or integrated with other memory devices, for example in a three dimensional stack, or in any one of several other possible expedients for integration known to those	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			skilled in the art to achieve a specific design, application, or economic goal. In the case of a DIMM, these on-module intermediary components are an on-DIMM Controller (CDC) 502 and an on-DIMM data manager (DMgr) 504**.** While the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well. CDC 502 and data manager DMgr 504 are operative to manage the interface between a non-volatile memory subsystem such as a Flash 506, a volatile memory subsystem such as a DRAM 508, and a host system represented by MCH 510.").	

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b. U.S. Patent Nos. 8,787,060/9,318,160

Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
'060: All asserted claims '160: All asserted claims	"array die"	Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification (that is, a die including memory cells); not indefinite; not subject to 35 U.S.C. § 112, ¶ 6.	'060, 1:57-62 ("In some cases, the control die 130 may include memory cells and therefore, also serve as an array die. . . . Alternatively, the control die 130 and the array dies 110 may be distinct elements and the control die 130 may not include any memory cells."); 1:53-56. '060, Abstract ("An apparatus is provided that includes a plurality of array dies and at least two die interconnects. The first die interconnect is in electrical communication with a data port of a first array die and a data port of a second array die and not in electrical communication with data ports of a third array die. The second die interconnect is in electrical communication with a data port of the third array die and not in electrical communication with data ports of the first array die and the second array die. The apparatus includes a control die that includes a first data conduit configured to transmit a data signal to the first die interconnect and not to the	Dictionary definition of "die" IEEE 100 The Authoritative Dictionary of IEEE Standards Terms (7th Ed. 2000), at 301 ("die (1) A single piece of silicon that contains one or more circuits and is or will be packaged as a unit."). McGraw-Hill Dictionary of Scientific and Technical Terms (6th Ed. 2003), at 595 ("[ELECTR] The tiny, sawed or otherwise machined piece of semiconductor material used in the construction of a transistor, diode, or other semiconductor device; plural is dice."). Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify that in the context of the '060/'160 patents, a person of ordinary skill in

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			second die interconnect, and at least a second data conduit configured to transmit the data signal to the second die interconnect and not to the first die interconnect.”). ’060 patent, 1:23-29 (“Memory modules may include a number of memory packages. Each memory package may itself include a number of array dies that are packaged together. Each array die may include an individual semiconductor chip that includes a number of memory cells. The memory cell may serve as the basic building block of computer storage representing a single bit of data.”). 1:33-42 (“FIG. 1A schematically illustrates a memory package 100 with three array dies 110 and a control die 130. The control die 130 is configured to respond to signals received by the memory package 100 by sending appropriate control signals to the array dies 110 and includes a driver 134 for driving data signals to each of the array dies 110 via a corresponding die interconnect 120. Further, the	the art would understand an “array die” refers to a die with memory cells and that the term is not indefinite. In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement. Specifically, Dr. Mangione-Smith will testify that a POSITA would understand that Rajan’s DRAM circuits are circuits with buffers and decoding circuitry ready to be packaged and as such they are just stacked, which differ from the interconnected array dies; and because Rajan’s DRAMs are stacked so differently from the claimed array dies, this difference in structure also renders Rajan’s control dies to have a significantly different structure and operation.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			control die 130 includes a driver 140 for driving command and/or address signals to each of the array dies 110 via another corresponding die interconnect 142."). 1:49-53 ("Each array die 110 also includes a chip select port 144, with the chip select ports 144 of the array dies 110 configured to receive corresponding chip select signals to enable or select the array dies for data transfer."); 1:57-62 ("In some cases, the control die 130 may include memory cells and therefore, also serve as an array die. Thus, as can be seen from FIG. lA, the control die 130 may also include a chip select port 144. Alternatively, the control die 130 and the array dies 110 may be distinct elements and the control die 130 may not include any memory cells."). 1:63-2:2 ("FIG. 1B schematically illustrates an example of a memory package 150 that includes four array dies 160 and a control die 170 that does	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			not include memory cells. As can be seen in FIG. 1B, each array die 160 includes a chip select port 174. However, because the control die 170 does not also serve as an array die, the control die 170 does not include a chip select port." 5:17-23 ("Although generally referred to as **array dies** herein, the **array dies** 210 may also be called slave dies or slave chips. Each of the **array dies** 210a-210d may include circuitry (e.g., memory cells) (not shown) for storing data. Examples of **array dies** compatible with certain embodiments described herein are described by the existing literature regarding the Hybrid Memory Cube (e.g., as cited above)."). '060, 23:62-24:5 ("a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, **each array die having data ports** ...."), '160, 23:47-24:3 ("stacked array dies including a first group of array dies and a second group of at least one array die").	

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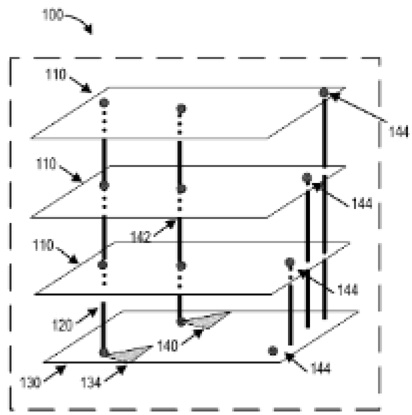
Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			 FIG. 1A	

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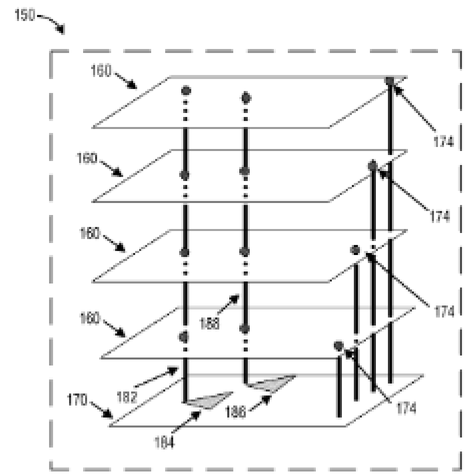
Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			 FIG. 1B	

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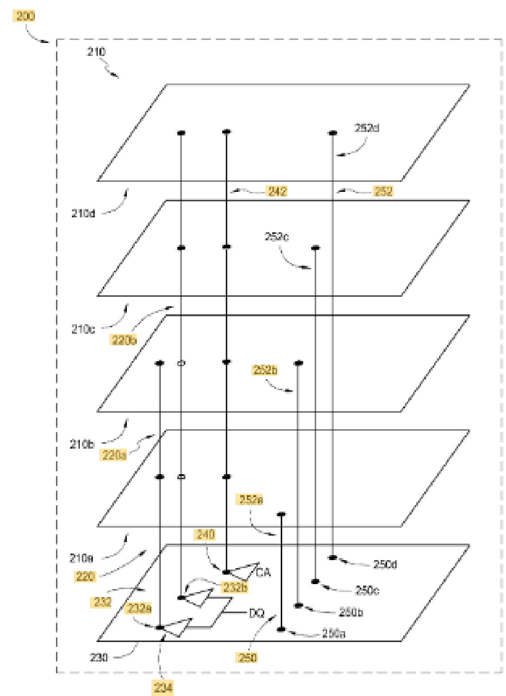
Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			 FIG. 2	

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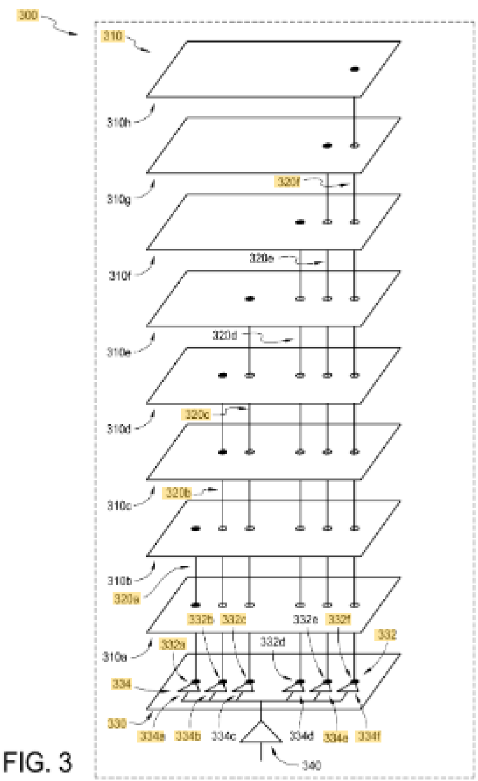
Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			 FIG. 3	

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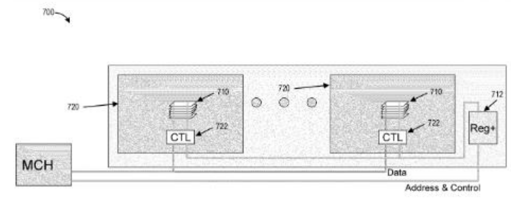
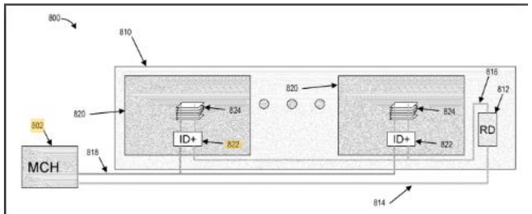
Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			 FIG. 7  FIG. 8 *See also id.*, 5:41-45, 5:46-62, 5:63-6:35, 10:18-34, 12:16-51, 18:38-19:7, 21:64-22:11. January 13, 2014 Netlist Response to Office Action for Patent App. 13/288,850, at 10 ("First of all, Rajan does not disclose 'a plurality of stacked array dies.' Rajan merely stacks DRAM circuits 206A-D, which are different from array dies. As a result, Rajan's buffer chip 202 also operates very differently from the control die in claim	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			1."); *see also, e.g.*, *id.* at 11 ("The Examiner further cites Paragraph [0044] [of Rajan] as disclosing the control die as recited in claim 1. . . . [T]he statements in this paragraph [0044] of Rajan says nothing about the existence of a first data conduit and a second data conduit in the buffer chip 202 and 'a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.' According to this paragraph [0044], all that is required of the buffer chip 202 is the capability of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system, and this requirement does not necessitate the use of a first data conduit and a second data conduit in the buffer chip 202 and 'a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.[¶] Furthermore, according to	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			paragraphs [0043] and [0044], this same capability of buffering the stack of DRAM circuits 206A-D to electrically and/or logically resemble at least one larger capacity DRAM circuit to the host system is required for each of the FIGS. 2A-2E, which show various configurations of a buffered stack of DRAM circuits 206A-D with the buffer chip 202. Since FIG. 2D of Rajan shows a single data bus between the buffer chip and all of the stacked DRAM circuits 206A-D (Rajan, paragraph [00511), this capability of buffering the stack of DRAM circuits 206A-D, which also applies to the configuration in FIG. 2D, can not be said to imply the existence of first and second data conduits in the buffer chip 202 and a control circuit controlling the respective states of the first data conduit and the second data conduit in response to any received control signals, because the first and second data conduits would be coupled to a same data line in the single data bus in FIG. 2D and it would make no sense to try to control respective states or the first data conduit and the second data conduit.'").	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			U.S. Patent Application Pub. No. 2008/0025137 to Rajan et al. ("Rajan 137"), [0018] ("For example, in various embodiments, one or more of the memory circuits 104A, 104B, 104N may include a monolithic memory circuit. For instance, such monolithic memory circuit may take the form of dynamic random access memory (DRAM). Such DRAM may take any form including, but not limited to synchronous (SDRAM), double data rate synchronous (DDR DRAM, DDR2 DRAM, DDR3 DRAM, etc.), quad data rate (QDR DRAM), direct RAMBUS (DRDRAM), fast page mode (FPM DRAM), video (VDRAM), extended data out (EDO DRAM), burst EDO (BEDO DRAM), multibank (MDRAM), synchronous graphics (SGRAM), and/or any other type of DRAM."), [0044] ("As shown in each of such figures, the buffer chip 202 is placed electrically between an electronic host system 204 and a stack of DRAM circuits 206A-D. In the context of the present description, a stack may refer to any collection of memory circuits."), [0071] ("A behavior of many DRAM circuits is specified by the	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			JEDEC standards and it may be desirable, in some embodiments, to exactly simulate a particular JEDEC standard DRAM. The JEDEC standard defines control signals thatf] a DRAM circuit must accept and the behavior of the DRAM circuit as a result of such control signals. For example, the JEDEC specification for a DDR2 DRAM is known as JESD79-2B."); *see also id.*, [0043], [0045], [0050]-[0051] and related figures, [0072].	
'060: 7	"The memory package of claim 1, wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect	Plain and ordinary meaning to a person of ordinary skill in the art in light of the specification; not indefinite.	'060, 2:8-15 ("Generally, a load exists on each of the drivers 134, 140, 184, and 186 by virtue of the drivers being in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies. Thus, to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power.").	Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify that in the context of the '060/'160 patents, a person of ordinary skill in the art would not view the claim as indefinite as Samsung has contended. In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement.

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	and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit, the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die.”		2:61-3:15 (“In certain embodiments, a method is provided for optimizing load in a memory package. The memory package comprises a plurality of array dies, at least a first die interconnect and a second die interconnect, and a control die. The control die comprises at least a first driver and a second driver, the first driver configured to drive a signal along the first die interconnect, and the second driver configured to drive the signal along the second die interconnect. The method comprises selecting a first subset of array dies of the plurality of array dies and a second subset of array dies of the plurality of array dies. The first subset of array dies and the second subset of array dies are exclusive of one another and are selected to balance a load on the first driver and on the second driver based at least in part on array die loads of array dies of the plurality of array dies and at least in part on die interconnect segment loads of segments of at least the first die interconnect and the second die interconnect. The method further comprises forming electrical connections between the first die interconnect and the first subset of array dies. In addition, the method comprises forming electrical connections between the second die interconnect and the second subset of array dies.”).	

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			’060, 16:42-55 (“FIG. 5 presents a flowchart for an example embodiment of a load optimization process 500. In certain embodiments, the load optimization process 500 may be performed, at least in part, by one or more computing systems. Further, the process 500, in some embodiments, may be used to optimize one or more loads in a memory package (e.g. memory package 200 or memory package 300). Optimizing the loads in the memory package can include optimizing the load on one or more conduits and/or drivers. As previously described with respect to FIGS. 2 and 3, the memory package can include a plurality of array dies, a plurality of die interconnects, and a control die. Furthermore, the control die can include a plurality of drivers, each of which may be configured to drive a signal along a die interconnect.”). 4:30-54 (“In certain embodiments, determining the number of die interconnects and the number of array dies in electrical communication with each die interconnect is based, at least in part, on a load of each array die and a load of the die interconnect that is in electrical communication with one or more of the array dies. [¶] In some	

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			embodiments, the load contribution from a die interconnect may be negligible compared to the load contribution from the array dies. In such embodiments, determining the number of die interconnects and the number of array dies in electrical communication with each die interconnect may be based, at least in part, on a load of each array die without considering the load of the die interconnect. However, as the physical size of a memory package shrinks, the load of a die interconnect becomes a non-negligible value relative to the load of the array dies. Thus, as memory packages become physically smaller, it becomes more important to consider the load of the die interconnect in determining the number of die interconnects and the number of array dies in electrical communication with each die interconnect. Advantageously, certain embodiments of the present disclosure account for both the loads of the array dies and the loads of the die interconnects on a conduit (e.g., driver) in determining the number of die interconnects to be used and the number of array dies in electrical communication with each die interconnect”)	

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			7:30-62 ("In some implementations, the difference between the load of the data conduit 232 a and the load of the data conduit 232 b is less than the maximum load for a data conduit as described above. Thus, in some cases, there may exist a degree of balance or equalization between the loads of the data conduits 232 a, 232 b. In some implementations, the difference between the load of the data conduit 232 a and the load of the data conduit 232 b is zero or substantially zero. In some embodiments, the length of each die interconnect 220, and the number of array dies 210 in electrical communication with each die interconnect 220 may be selected to maintain the difference between the load of the data conduit 232 a and the load of the data conduit 232 b to be at or below a threshold load difference. For example, suppose that the load of each array die 210 is 1, the load of each segment of the die interconnects 220 is 0.25, and that the threshold load difference is 0.5. Using the configuration schematically illustrated in FIG. 2, the load on the data conduit 232 a in this example is 2.5 and the load on the data conduit 232 b in this example is 3. Thus, in this example, the difference between the load of the data conduit 232 a and the load of the data	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			conduit 232 b is at the threshold load difference value of 0.5. However, an alternative configuration that places the die interconnect 220 a in electrical communication with only the array die 210 a, and the die interconnect 220 b in electrical communication with the array dies 210 b-210 d would not satisfy the threshold load difference value of 0.5 of the above example. In the alternative configuration, the load on the data conduit 232 a would be 1.25 and the load on the data conduit 232 b would be 4. Thus, in the alternative configuration, the difference between the load of the data conduit 232 a and the load of the data conduit 232 b is 2.75, which is above the threshold load difference value of 0.5."); *see also* 11:41-60, 14:4-21, 14:22-46, 17:4-23.	
'060: 6, 11-14, 16-19, 20, 21, 23-28.	"chip select signal"/ "chip select conduits"	"chip select signal": a signal for enabling or selecting one or more array dies for data transfer.	'060 patent, 1:49-56 ("Each array die 110 also includes a chip select port 144, with the chip select ports 144 of the array dies 110 configured to receive corresponding chip select signals to enable or select the array dies for data transfer. The array dies 110 are configured to transfer data (e.g. read or	Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify that in the context of the '060/'160 patents, a "chip select signal" is a

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		"chip select conduits": conduit for transmitting "chip select signals," as construed above.	write) to or from the selected memory cells identified by the command, address, and chip select signals via the die interconnects."). *Id.*, 1:53-56 ("The array dies 110 are configured to transfer data (e.g. read or write) to or from the selected memory cells identified by the command, address, and chip select signals via the die interconnects."). *Id.* at 4:49-54 ("Advantageously, certain embodiments of the present disclosure account for both the loads of the array dies and the loads of the die interconnects on a conduit (e.g., driver) in determining the number of die interconnects to be used and the number of array dies in electrical communication with each die interconnect."); *Id.* at 9:46-60 ("In addition, in certain embodiments, the control die 230 may include a plurality of chip select conduits 250 (e.g., chip select conduits 250 a-250 d as shown in FIG. 2).	signal for enabling or selecting one or more array dies for data transfer; and a "chip select conduit" is a conduit for providing a chip select signal to a corresponding array die. In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			Further, the control die 230 may include corresponding die interconnects 252 (e.g., die interconnects 252 a-252 d) with one die interconnect 252 in electrical communication with one chip select conduit 250 and one array die 210. . . . Each of the chip select conduits 250 may be configured to provide a chip select signal to a corresponding array die 210 via a corresponding die interconnect 252."). *Id.*, 10:56-67 ("In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few. Further, as the signal is not limited to a data signal, in some embodiments, the conduits 332 may include conduits configured to provide signals other than data signals to the die interconnects 320. For example, the conduits may include conduits configured to provide a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal to one or more die interconnects. Consequently, in some embodiments, the drivers 334	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			may be configured to drive signals other than data signals.”). *Id.*, 15:48-54 (“In some embodiments, the driver structure 400 is bi-directional. In such embodiments, operation of the drivers 404a and 404b, and 408a and 408b may be controlled or enabled by a control signal (e.g., a directional control signal). This control signal, in some cases, may correspond to one or more of a command/address signal (e.g., read/write) and a chip select signal.”). *Id.*, 16:21-28 (“In some embodiments, one or more chip selects, as illustrated in FIG. 2, may be used to select, determine, or enable the array die that communicates the signal to or from one or more of the conduits 406a and 406b and the drivers 408a and 408b. Similarly, in some embodiments, the chip select may select, determine, or enable the array die to receive and/or respond to the signal driven by the drivers 404a and 404b to the array dies.”).	

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c. U.S. Patent No. 10,860,506

Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
1-3, 11, 15, 16	"one or more previous operations"	one or more previous memory operations. (Note: this proposed construction is not intended to limit the recited "operations" to ones involving writing to or reading from a DRAM).	'506 patent, 3:29-34 ("The memory module is operable to perform memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module."). *Id.*, 4:9-19 ("Further, in one embodiment, each buffer circuit includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit and a time when a strobe or data signal is received from the memory controller. This time interval is used during a subsequent read operation to time transmission of read data to the memory controller, such that the read data arrives at the memory controller within a time limit in accordance with a read latency parameter associated with the memory	Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify that in the context of the '506 patent, a person of ordinary skill in the art would understand "previous operations" means "previous memory operations." In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement. JESD 79-3C, DDR3 SDRAM (2008) (IPR2022-00711), Section 4.1, Command Truth Table. *Id.*, Section 4.8 Write Leveling ("During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to exit write leveling mode"). JESD 79-3C, at 34 ("The No Operation command should be used in cases when the

Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			system."). *Id.*, 10:11-21 ("In one embodiment, each isolation devices includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit 116 and a time when a write strobe or write data signal is received from the MCH 101. This time interval is used during a subsequent read operation to time the transmission of read data to the MCH 101, such that the read data follows a read command by a read latency value associated with the system 100, as explained in more detail below.") *Id.*, FIGs. 12A-12B and accompanying description at 15:27-16:24 ("FIG. 12A is a timing diagram for a write operation according to one embodiment. As shown, after a write command W/C associated with the write operation is received by the module control circuit **116** at time t1,	DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from register[i]ng any unwanted commands **between operations**. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle."). *Id.* ("The No OPeration (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (CS# LOW and RAS#, CAS#, and WE# HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected."). *Id.*, Figs. 18-19 (timing diagrams for write leveling operation illustrating how system memory controller sends consecutive NOP commands to ensure that the memory controller does not issue any other memory operations during write leveling).

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			the module control circuit **116** outputs one or more enable signals EN at time t2 in response to the write commands. The one or more enable signals are received by an isolation device **118** at time t3, which afterwards receives one or more strobe signal DQS from the MCH **101** at time t4. Note that the same enable signal may be received by another isolation device **118** at time t3′, which can be in a different cycle of the system clock MCK from the cycle which t3 is in. The time interval between t4 and t1 is consistent with a write latency W.L. associated with the system **100**, and is controllable by the MCH **101** and knowable to the isolation device **118**. The time interval between t4 and t3, referred to hereafter as an enable-to-write data delay EWD, can be determined by the isolation device **118** since both these signals are received by the isolation device. Based on such determination, the isolation device **118** can have knowledge of the time interval between t3 and t1, referred to hereafter as a command-to-enable delay CED, which can be used by the isolation	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			device **118** to properly time transmission of read data to the MCH, as explained further below.[¶] FIG. 12B is a timing diagram for a read operation according to one embodiment. As shown, after a read command R/C associated with the read operation is received by the module control circuit **116** at time t5, the module control circuit **116** outputs one or more enable signals EN at time t6 in response to the read commands. The one or more enable signals are received by an isolation device **118** at time t7, which afterwards receives at time t8 read data signals (not shown) and one or more strobe signal DQS from the respective group of memory devices. . . . [¶] With knowledge of the time interval between t7 and t5, which should be about the same as the time interval between t3 and t1, i.e., the command-to-enable delay CED, in certain embodiments, the isolation device can add a proper amount of delay to the read data signals and the one or more DQS signal such that the read data signals and the one or more DQS signal are transmitted at time t9	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			by the isolation device to the MCH **101** via the respective group of data/strobe signal lines **130**, with the time interval between t9 and t5 being consistent with a read latency R.L. associated with the system **100**. [¶] The time interval between t4 and t3, i.e., the enable to write data delay EWD, is determined by the delay control circuit **650** in the ID control circuit **310**, as shown in FIG. 6. According to one embodiment, as shown in FIG. 13, the delay control circuit **650** includes a preamble detector **1310** to detect a write preamble in the DQS, a flip-flop circuit **1320** having an enable input EN receiving one of the module control signals and a clock input CK receiving the buffered module clock signal CK**0**, and a counter circuit **1330** having a Start input receiving the one of the module control signals, a Stop input receiving an output of the flip-flop circuit **1320**. Thus, the output of the counter circuit, i.e., the delay signal DS, would indicate a time interval from when the write preamble is detected and when	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			the one of the module control signal is received."). *Id.*, FIG. 18 and accompanying description at 18:29-40 ("Since the time interval between the arrival of the command signals from the MCH 101 and the arrival of the write data/strobe signal DQ/DQS from the MCH 101 is a set according to a write latency parameter associated with the system 100, the time interval EWD can be used to ascertain a time interval CED between the time when a command signal is received by the memory module 110 and the time when the one or more enable signals are received by the isolation device 118. The time interval CED can be used by the isolation device 118 to properly time the transmission of read data to the MCH 101, as described above and explained further below.").	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
14	"[the method further comprising,] before receiving the input C/A signals corresponding to the memory read operation, determining the first predetermined amount based at least on signals received by the first data buffer"	the step of determining the first predetermined amount based at least on signals received by the first data buffer occurs before the earlier recited step of "receiving, at the module device, input C/A signals corresponding to a memory read operation via the C/A signal lines."	'506 patent, Fig. 18 and accompanying description at 18:6-64 ("Thus, as shown in FIG. 18, in one embodiment, a memory module 110 operates in the memory system 100 according to a method 1800. In the method, during a write operation, one or more module control signals are received by an isolation device 118 from a module control circuit or module controller 116 (1810). The module controller 116 generates the one or more module control signals in response to C/A signals representing a write command from the MCH 101. The one or more module control signals are used to control the isolation device 118. For example, the one or more module control signals may include one or more first enable signals to enable a write path to allow write data be communicated to a selected subgroup of memory devices among the group of memory devices coupled to the isolation device 118. After a time interval from receiving the one or more first enable signals, write data DQ and write strobe DQS are received by the isolation device	Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify that in the context of the '506 patent, a person of ordinary skill in the art would understand claim 14 is not indefinite. In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			118 from the MCH 101 (1820). In one embodiment, upon receiving the one or more first enable signal, a counter is started, which is stopped when the write data DQ or write strobe DQS is received. Thus, a time interval EWD between receiving the one or more first enable signals and receiving the write strobe signal DQS is recorded.[¶] Since the time interval between the arrival of the command signals from the MCH 101 and the arrival of the write data/strobe signal DQ/DQS from the MCH 101 is a set according to a write latency parameter associated with the system 100, the time interval EWD can be used to ascertain a time interval CED between the time when a command signal is received by the memory module 110 and the time when the one or more enable signals are received by the isolation device 118. The time interval CED can be used by the isolation device 118 to properly time the transmission of read data to the MCH 101, as described above and explained further below.[¶] As shown in FIG. 18, a delay signal DS is generated	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			according to the time interval EWD (1830). Concurrent to receiving the write strobe signal DQS, the isolation device 118 also receives a set of write data signals DQ (1840). The received write data signals are transmitted to the subgroup of memory devices (1850), which are selected from the group of memory devices coupled to the isolation device 118 by the one or more first enable signals.[¶] During a read operation, another set of module control signals including, for example, one or more second enable signals, are received by the isolation device 118 from the module controller 116 (1860). The one or more second enable signals are generated by the module controller 116 in response to read command signals received from the MCH 101, and are used by the isolation device 118 to select a subgroup of memory devices from which to receive read data. Afterwards, a read strobe signal DQS and a set of read data signal DQ are received from the selected subgroup of memory devices (1870). To properly time the transmission of the DQS and	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			DQ signals to the MCH 101, the DQS and DQ signals are adjusted (e.g., delayed) according to the delay signal DS, such that the DQS and DQ signals follow a read command by a time interval consistent with a read latency parameter associated with the system 100."). *See also*, *id.*, 3:29-34, 4:9-19, 10:11-21, 15:27-16:24, FIGs. 12A-12B.	

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d. U.S. Patent No. 10,949,339

Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
1	"wherein the byte-wise data path is enabled for a first <u>time period in accordance with a latency parameter</u> to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period"	"time period in accordance with a latency parameter" means a time period wherein both the start of the time period and duration of the time period depends on at least a latency parameter. The remaining term requires no additional construction at this time (i.e., plain and ordinary meaning).	'339 patent, 15:61-16:6 ("As is known, Column Address Strobe (CAS) latency is a delay time which elapses between the moment the memory controller 420 informs the memory modules 402 to access a particular column in a selected rank or row and the moment the data for or from the particular column is on the output pins of the selected rank or row. The latency may be used by the memory module to control operation of the data transmission circuits 416. During the latency, address and control signals pass from the memory controller 420 to the control circuit 430 which produces controls sent to the control logic circuitry 502 (e.g., via lines 432) which then controls operation of the components of the data transmission circuits 416."). *Id.*, 16:7-11 ("For a write operation, during the CAS latency, the control circuit 430, in one embodiment, provides enable control signals to the control logic circuitry 502 of each data transmission circuit 416, whereby the control logic circuitry 502 selects either path A or path B to direct the data."); 16:11-25. *Id.*, FIG. 6 and accompanying description at 17:45-18:11 ("Operation of a memory module	Dictionary definition for "period" Webster's New World, College Dictionary (4th Ed., 2000) at 1071 (period: "2. The interval between certain happenings *[*a ten-year *period* of peace*]*" 3. A portion of time, often indefinite, characterized by certain events, processes, conditions, etc.; state *[a period* of change, the present *period]*"). Dictionary definition for "latency" Wiley Electrical and Electronics Engineering Dictionary (2004), at 532 ("1. The time interval that elapses between the request or triggering of an action, and the obtaining of the desired result, or completion.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			using the data transmission circuit 416 may be further understood with reference to FIG. 6, an illustrative timing diagram of signals of the memory module 402. The timing diagram includes first through eighth time periods 601-608. When the memory devices 404 are synchronous memories, each of the time periods 601-608 may correspond to one clock cycle of the memory devices 404. The first, second, and third time periods 601-603 illustrate write operations with data passing from the memory controller 401 to the memory module 402. The fourth time period 604 is a transition between the write operations and subsequent read operations. The timing diagram shows a write operation to the first group of memory devices 412A, 412C connected to the first terminals Y1 of the data transmission circuits 416 and a write operation to the second group of memory devices 412B, 412D connected to the second terminals Y2 of the data transmission circuits 416. Recalling the CAS latency described above, each write operation extends over two time periods in a pipelined manner. The write to the first group of memory devices 412A, 412C appears in the first time period 601 when system address and control signals 440 pass from the memory controller 420 to the	2. The time interval that elapses between initiating a request for data and the transfer of said data."). Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify how a person of ordinary skill in the art would understand "time period in accordance with a latency parameter" in the context of the '339 patent. In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			module controller 430. The control circuit 430 evaluates the address and control signals 440 to determine that data is to be written to memory devices 412A, 412C in the first group. During the second time period 602, the control circuit 430 supplies control signals to the control logic circuitry 502 to enable the first tristate buffer 504 and to disable the second tristate buffer 506 and the read buffer 509. Thus, during the second time period 602, data bits pass from the data lines 518 to the first terminal Y1 and on to the memory devices 412A, 412C."). U.S. 7,532,537, 21:28-53 ("In certain embodiments, the circuit 40 comprises the SPD device 240 which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device 240 of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit 40. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			ranks of memory devices 30 from the memory controller 20. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device 240 does not utilize this extra cycle of time.").	
11	"each respective data transmission circuit is configurable to enable the data paths for a first <u>time period in accordance with a latency parameter</u>	"time period in accordance with a latency parameter" as defined above. The remaining term requires no additional construction at this	*See* above.	*See* above.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	to actively drive a respective section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period"	time (i.e., plain and ordinary meaning).		
34	"wherein the first set of tristate buffers are enabled for the first time period in accordance with a latency parameter"	"time period in accordance with a latency parameter" as defined above. The remaining term requires no additional construction at this time (i.e., plain and ordinary meaning).	*See* above.	*See* above.
35	"wherein the second set of tristate buffers are enabled for the second time period in	"time period in accordance with a latency parameter" as defined above.	*See* above.	*See* above.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	<u>accordance with a latency parameter"</u>	The remaining term requires no additional construction at this time (i.e., plain and ordinary meaning).		
1	"each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals"	No construction required (plain and ordinary meaning to a person of ordinary skill in the art in light of the specification); not subject to 35 U.S.C. § 112, ¶ 6.	'339, claim 1 ("wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period; and wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period"). '339, Abstract ("The memory module further comprises a plurality of byte-wise buffers controlled by the set of module control signals to actively drive respective byte-wise sections	Dictionary definition of "buffer" Comprehensive Dictionary of Electrical Engineering (2nd Ed., 2005), at 85 ("buffer[:] a temporary data storage area in memory that compensates for the different speeds at which different elements are transferred within a system. Buffers are used when data transfer rates and/or data processing rates between sender and receiver vary, for instance, a printer buffer, which is necessary because the computer sends data to the printer faster than the data can be physically printed.").

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			of each data signal associated with the read or write operation between the memory controller and the selected rank”). *Id.*, Fig. 5 and accompanying description at 15:26-33 (“FIG. 5 schematically illustrates an example data transmission circuit 416 compatible with certain embodiments described herein. In one embodiment, the data transmission circuits 416 includes control logic circuitry 502 used to control the various components of the data transmission circuit 416, which may include one or more buffers, one or more switches, and one or more multiplexers among other components.”). *Id.*, 8:31-53 (“The plurality of data transmission circuits 416, 416′ is configurable to be operatively coupled to the system memory controller 420, 420′ and configurable to receive module control signals from the control circuit 430, 430′. At least one first data transmission circuit of the plurality of data transmission circuits 416, 416′ is operatively coupled to at least two memory devices of the plurality of memory devices 412, 412′. At least one second data transmission circuit of the plurality of data transmission circuits 416, 416′ is operatively coupled to at least two memory devices of the plurality of memory devices 412, 412′. The at	Dictionary definition of “logic” IEEE 100 The Authoritative Dictionary of IEEE Standards Terms (7th Ed. 2000), at 636 (“(B) Pertaining to the type or physical realization of logic elements used, for example, diode logic, and logic.”). Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify how a person of ordinary skill in the art would understand the term in the context of the ’339 patent, and that the ’339 patent provides detailed description on the structure and function of a byte-wise buffer as well the logic within the buffer. In addition, if the expert disagrees with

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			least one first data transmission circuit is configurable to respond to the module control signals by selectively allowing or inhibiting data transmission between the system memory controller 420, 420′ and at least one selected memory device of the at least two memory devices operatively coupled to the at least one first data transmission circuit. The at least one second data transmission circuit is configurable to respond to the module control signals by selectively allowing or inhibiting data transmission between the system memory controller 420, 420′ and at least one selected memory device of the at least two memory devices operatively coupled to the at least one second data transmission circuit.”). *Id.*, 14:15-18 (“In certain embodiments, by having the data transmission circuit 416 comprise or serve as a “byte-wise” buffer (e.g., as shown in the examples of FIGS. 4A and 4B), the data signals are synchronous with the synch clock.”); *id.*, 13:31-36 (“In certain embodiments, the data transmission circuit 416 comprises or functions as a byte-wise buffer. In certain such embodiments, each of the one or more data transmission circuits 416 has the same bit width as does the associated memory devices 412 per rank to which the data transmission circuit 416 is operatively	any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement. For example, Dr. Mangione-Smith may opine why it is improper to import a “fork-in-the-road” requirement into the term.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			coupled."); *id.*, 13:36-14:14, FIGs. 4A, 4B. Description of "byte-wise buffer"/"transmission circuit" (416/416'): 10:54-13:30; 14:18-33, 14:34-55. 13:31-53 ("In certain embodiments, the data transmission circuit 416 comprises or functions as a byte-wise buffer. In certain such embodiments, each of the one or more data transmission circuits 416 has the same bit width as does the associated memory devices 412 per rank to which the data transmission circuit 416 is operatively coupled. For example, as schematically illustrated by FIG. 4A (which corresponds generally to FIG. 3A), the data transmission circuit 416 can be operatively coupled to a single memory device 412 per rank, and both the data transmission circuit 416 and the memory device 412 per rank to which the data transmission circuit 416 is operatively coupled can each have the same bit width (e.g., 4 bits, 8 bits, or 16 bits). The data transmission circuit 416 of FIG. 4A has a bit width of 8 bits, and receives data bits 0-7 from the system memory controller 420 and selectively transmits the data bits 0-7 to selected memory devices 412A, 412B, 412C, 412D in response to the module control signals from the control	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			circuit 430. Similarly, data transmission circuits 416' of certain embodiments can function as byte-wise buffer for associated memory devices 412'A, 412'B, 412'C, 412'D to which the data transmission circuits 416' are operatively coupled in response to the module control signals from the control circuit 430""). 13:54-14:25 ("In certain other embodiments, the bit widths of one or more of the memory devices 412 may be different from the bit widths of the one or more data transmission circuits 416 to which they are connected. For example, as schematically illustrated by FIG. 4B (which corresponds generally to FIG. 3B), the data transmission circuits 416 may have a first bit width (e.g., a bit width of 8 bits) and the memory devices 412 may have a second bit width which is less than the first bit width (e.g., one-half the first bit width, or a bit width of 4 bits), with each data transmission circuit 416 operatively coupled to multiple memory devices 412 per rank (e.g., two memory devices 412 in each rank). In certain such embodiments, the total bit width of the multiple memory devices 412 per rank connected to the circuit 416 equals the bit width of the circuit 416 (e.g., 4 bits, 8 bits, or 16 bits). The data transmission circuit 416 of FIG. 4B has a total bit width of 8 bits, and receives data bits 0-7 from the system	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			memory controller 420 and selectively transmits data bits 0-3 to a first memory device 412A1, 412B1, 412Ci, 412D1 and data bits 4-7 to a second memory device 412A2 , 412B2 , 412C2 , 412D2 in response to the module control signals from the control circuit 430. Similarly, data transmission circuits 416' of certain embodiments can function with different bit widths than those of the associated memory devices 412'A1 , 412'A2 , 4121B1 , 4121B2 , 412'Ci, 412'C2 , 412'D1, 412'D2 to which the data transmission circuits 416' are operatively coupled in response to the module control signals from the control circuit 430""). Description regarding the logic within the buffer: 10:43-46, 15:26-40 ("FIG. 5 schematically illustrates an example data transmission circuit 416 compatible with certain embodiments described herein. In one embodiment, the data transmission circuits 416 includes control logic circuitry 502 used to control the various components of the data transmission circuit 416, which may include one or more buffers, one or more switches, and one or more multiplexers among other components. The illustrated embodiment of FIG. 5 is 1-bit wide and switches a single data line 518 between the	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			memory controller 420 and the memory devices 412. In other embodiments, the data transmission circuit 416 may be multiple bits wide, for example, 8 bits, and switch a corresponding number of data lines 518. In a multiple bit wide embodiment, the control logic circuitry 502 may be shared over the multiple bits."); 15:61-16:6 ("As is known, Column Address Strobe (CAS) latency is a delay time which elapses between the moment the memory controller 420 informs the memory modules 402 to access a particular column in a selected rank or row and the moment the data for or from the particular column is on the output pins of the selected rank or row. The latency may be used by the memory module to control operation of the data transmission circuits 416. During the latency, address and control signals pass from the memory controller 420 to the control circuit 430 which produces controls sent to the control logic circuitry 502 (e.g., via lines 432) which then controls operation of the components of the data transmission circuits 416."); 17:14-44 ("Referring again to FIG. 3A, when the memory controller 420 executes read or write operations, each specific operation is	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			targeted to a specific one of the ranks A, B, C, and D of a specific memory module 402. The data transmission circuit 416 on the specifically targeted one of the memory modules 402 functions as a bidirectional repeater/multiplexor, such that it drives the data signal when connecting from the system memory controller 420 to the memory devices 412. The other data transmission circuits 416 on the remaining memory modules 402 are disabled for the specific operation. For example, the data signal entering on data line 518 entering into data transmission circuit 416 is driven to memory devices 412A and 412C or 412B and 412C depending on which memory devices are active and enabled. The data transmission circuit 416 then multiplexes the signal from the memory devices 412A, 412B, 412C, 412D to the system memory controller 420. The data transmission circuits 416 may each control, for example, a nibble-wide data path or a bytewide-data path. As discussed above, the data transmission circuits 416 associated with each module 402 are operable to merge data read signals and to drive data write signals, enabling the proper data paths between the system memory controller 420 and the targeted or selected memory devices 412. Thus, the memory controller 420, when there are four four-rank memory modules, sees four	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			load-reducing switching circuit loads, instead of sixteen memory device loads. The reduced load on the memory controller 420 enhances the performance and reduces the power requirements of the memory system, as compared with, for example, the conventional systems described above with reference to FIGS. 1A, 1B and 2A-2D."); 15:13-18, 16:7-18:65; Figs. 5-6. *See also id.*, 14:34-55 ("One or more of the data transmission circuits 416, in accordance with an embodiment of this disclosure, is operatively coupled to a corresponding one or more of the data lines 452 connected to one or more memory devices 412 in each of the ranks A, B, C, D. For example, in certain embodiments, each data transmission circuit 416 is connected to one or more data lines 452 connected to one corresponding memory device in each of the ranks (e.g., memory devices 204A, 204B, 204C, and 204D, as shown in FIG. 3A). Each data line 450, 452 thus carries data from the system memory controller 420, through the data transmission circuits 416, to the memory devices 204A, 204B, 204C, 204D connected to the data transmission circuits 416. The data transmission circuits 416 of certain embodiments may be used to drive each data bit to and from the memory controller 420 and the	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			memory devices 412, instead of the memory controller 420 and the memory devices 412 directly driving each data bit to and from the memory controller 420 and the memory devices 412. Specifically, as described in more detail below, one side of each data transmission circuit 416 of certain embodiments is operatively coupled to a memory device 412 in each rank (e.g., via data lines 452), while the other side of the data transmission circuit 416 is operatively coupled to the corresponding data line 450 of the memory controller 420."). *See also*, *id.*, 10:54-11:4 ("In certain embodiments, at least one memory module 402, 402′ comprises a plurality of data transmission circuits 416, 416′ mounted on the one or more PCBs 410, 410′, within the one or more PCBs 410, 410′, or both on and within the one or more PCBs 410, 410′. The plurality of data transmission circuits 416, 416′ are operatively coupled to the control circuit 430, 430′ (e.g., via lines 432, 432′), and configured to be operatively coupled to the system memory controller 420, 420′ (e.g., via the data lines 450, 450′) upon operatively coupling the memory module 402, 402′ to the computer system. In certain embodiments, these data transmission circuits 416, 416′ can be referred to as "load-reducing circuits" or "load-reducing switching	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			circuits." As used herein, the terms "load-reducing" or "load-reducing switching" refer to the use of the data transmission circuits 416, 416′ to reduce the load seen by the system memory controller 420, 420′ when operatively coupled to the memory module 402, 402′.).	
1	"logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period"	"N-bit wide write data" means "write data that is N bits in width"; no other terms requires construction; not indefinite; not subject to 35 U.S.C. § 112, ¶ 6.	*See* above; *see also* '339 patent, 15:61-16: ("As is known, Column Address Strobe (CAS) latency is a delay time which elapses between the moment the memory controller 420 informs the memory modules 402 to access a particular column in a selected rank or row and the moment the data for or from the particular column is on the output pins of the selected rank or row. The latency may be used by the memory module to control operation of the data transmission circuits 416. During the latency, address and control signals pass from the memory controller 420 to the control circuit 430 which produces controls sent to the control logic circuitry 502 (e.g., via lines 432) which then controls operation of the components of the data transmission circuits 416."); *Id.*, 16:7-44 ("For a write operation, during the CAS latency, the control circuit 430, in one embodiment, provides enable control signals to	*See* above.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			the control logic circuitry 502 of each data transmission circuit 416, whereby the control logic circuitry 502 selects either path A or path B to direct the data. Accordingly, when the control logic circuitry 502 receives, for example, an "enable A" signal, a first tristate buffer 504 in path A is enabled and actively drives the data value on its output, while a second tristate buffer 506 in path B is disabled with its output in a high impedance condition. In this state, the data transmission circuit 416 allows the data to be directed along path A to a first terminal Y1, which is connected to and communicates only with the first group of the memory devices 412, e.g., those in ranks A and C. Similarly, if an "enable B" signal is received, the first tristate 504 opens path A and the second tristate 506 closes path B, thus directing the data to a second terminal Y2, which is connected to and communicates only with the second group of the memory devices 412, e.g., those in ranks B and D. [¶] For a read operation, the data transmission circuit 416 operates as a multiplexing circuit. In the illustrated embodiment of FIG. 5, for example, data signals read from the memory devices 412 of a rank are received at the first or second terminals Y1, Y2 of the data transmission circuit 416. The data signals are fed to a multiplexer 508, which selects one to route to its output. The control	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			logic circuitry 502 generates a select signal to select the appropriate data signal, and the selected data signal is transmitted to the system memory controller 420 along a single data line 518, preferably after passing through a read buffer 509. The read buffer 509 may be a tristate buffer that is enabled by the control logic circuitry 502 during read operations. In another embodiment, the multiplexer 508 and the read buffer 509 may be combined in one component. In yet another embodiment, the multiplexer 508 and the read buffer 509 operations may be split over two tristate buffers, one to enable the value from Y1 to the data line 518 and another to enable the value from Y2 to the data line 518."). FIG. 6 and accompanying description at 17:66-18:65 ("The first, second, and third time periods 601-603 illustrate write operations with data passing from the memory controller 401 to the memory module 402. The fourth time period 604 is a transition between the write operations and subsequent read operations. The timing diagram shows a write operation to the first group of memory devices 412A, 412C connected to the first terminals Y1 of the data transmission circuits 416 and a write operation to the second group of memory devices 412B, 412D connected to the second terminals Y2 of	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			the data transmission circuits 416. Recalling the CAS latency described above, each write operation extends over two time periods in a pipelined manner. [¶] The write to the first group of memory devices 412A, 412C appears in the first time period 601 when system address and control signals 440 pass from the memory controller 420 to the module controller 430. The control circuit 430 evaluates the address and control signals 440 to determine that data is to be written to memory devices 412A, 412C in the first group. During the second time period 602, the control circuit 430 supplies control signals to the control logic circuitry 502 to enable the first tristate buffer 504 and to disable the second tristate buffer 506 and the read buffer 509. Thus, during the second time period 602, data bits pass from the data lines 518 to the first terminal Y1 and on to the memory devices 412A, 412C. [¶] Similarly, the write to the second group of memory devices 412A, 412C appears in the second time period 602 when system address and control signals 440 pass from the memory controller 420 to the control circuit 430. The control circuit 430 evaluates the address and control signals 440 to determine that data is to be written to memory devices 412B, 412D in the second group. During the third time period 603, the control circuit 430 supplies control signals	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			to the control logic circuitry 502 to enable the second tristate buffer 506 and to disable the first tristate buffer 504 and the read buffer 509. Thus, during the third time period 603, data bits pass from the data lines 518 to the second terminal Y2 and on to the memory devices 412B, 412D. [¶] The fifth, sixth, seventh, and eighth time periods 605-608 illustrate read operations with data passing to the memory controller 420 from the memory module 402. The timing diagram shows a read operation from the first group of memory devices 412A, 412C connected to the first terminals Y1 of the data transmission circuits 416 and a read operation from the second group of memory devices 412B, 412D connected to the second terminals Y2 of the data transmission circuits 416. Recalling the CAS latency described above, each read operation extends over two time periods in a pipelined manner. [¶] The read from the first group of memory devices 412A, 412C appears in the fifth time period 605 when system address and control signals 440 pass from the memory controller 420 to the control circuit 430. The control circuit 430 evaluates the address and control signals 440 to determine that data is to be read from memory devices 412A, 412C in the first group. During the sixth time period 606, the control circuit 430 supplies control signals to the control logic circuitry 502	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			to cause the multiplexer 58 to select data from the first terminal Y1, to enable the read buffer 509, and to disable the first tristate buffer 504 and the second tristate buffer 506. Thus, during the sixth time period 606, data bits pass from the memory devices 412A, 412C via the first terminal Y1 to data lines 518 and on to the memory controller 420. [¶] The read from the second group of memory devices 412B, 412D appears in the seventh time period 607 when system address and control signals 440 pass from the memory controller 420 to the control circuit 430. The control circuit 430 evaluates the address and control signals 440 to determine that data is to be read from memory devices 412B, 412D in the second group. During the eighth time period 608, the control circuit 430 supplies control signals to the control logic circuitry 502 to cause the multiplexer 508 to select data from the second terminal Y2, to enable the read buffer 509, and to disable the first tristate buffer 504 and the second tristate buffer 506. Thus, during the eighth time period 606, data bits pass from the memory devices 412B, 412D via the second terminal Y2 to data lines 518 and on to the memory controller 420.”). *Id.*, Figs. 5-6.	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
11	"the respective data transmission circuit in response to the module control signals is configured to enable a first subset of the first tristate buffers to drive the first subsection of the respective section of the N-bit wide write data to a first subset of the respective module data lines coupled to a first one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks, and to enable a second subset of the first tristate buffers to drive a second subsection of the respective	No construction required (plain and ordinary meaning to a person of ordinary skill in the art in light of the specification); not indefinite; not subject to 35 U.S.C. § 112, ¶ 6.	*See* above; *see also* '339, Fig. 5 and accompanying description at 15:26-33 ("FIG. 5 schematically illustrates an example data transmission circuit 416 compatible with certain embodiments described herein. In one embodiment, the data transmission circuits 416 includes control logic circuitry 502 used to control the various components of the data transmission circuit 416, which may include one or more buffers, one or more switches, and one or more multiplexers among other components."). *Id.*, 8:31-53 ("The plurality of data transmission circuits 416, 416′ is configurable to be operatively coupled to the system memory controller 420, 420′ and configurable to receive module control signals from the control circuit 430, 430′. At least one first data transmission circuit of the plurality of data transmission circuits 416, 416′ is operatively coupled to at least two memory devices of the plurality of memory devices 412, 412′. At least one second data transmission circuit of the plurality of data transmission circuits 416, 416′ is operatively coupled to at least two memory devices of the plurality of memory devices 412, 412′. The at least one first data transmission circuit is configurable to respond to the module control signals by selectively allowing or inhibiting	Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify how a person of ordinary skill in the art would understand the term in the context of the '339 patent, and that the '339 patent provides detailed description on the transmission circuit, the logic within the transmission circuit and how the tristate buffers are enabled and data paths are controlled to drive the write data to the respective module data lines. In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement. For example, Dr. Mangione-Smith may opine why it is improper to

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	section of the N-bit wide write data to a second subset of the respective module data lines coupled to a second one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks"		data transmission between the system memory controller 420, 420′ and at least one selected memory device of the at least two memory devices operatively coupled to the at least one first data transmission circuit. The at least one second data transmission circuit is configurable to respond to the module control signals by selectively allowing or inhibiting data transmission between the system memory controller 420, 420′ and at least one selected memory device of the at least two memory devices operatively coupled to the at least one second data transmission circuit."). *See* citations for "data transmission circuit," "byte-wise buffers" and "logic" above.	import a "fork-in-the-road" requirement into the term.
19	"each respective buffer further includes logic configurable to enable the data paths for a first time period to actively drive a respective section of the first N-bit wide data associated with the first memory operation from	No construction required (plain and ordinary meaning to a person of ordinary skill in the art in light of the specification); not indefinite; not subject to 35 U.S.C. § 112, ¶ 6.	*See* citations for "data transmission circuit," "byte-wise buffers" and "logic" above; *see also* 16:26-44 ("For a read operation, … The control logic circuitry 502 generates a select signal to select the appropriate data signal, and the selected data signal is transmitted to the system memory controller 420 along a single data line 518, preferably after passing through a read buffer 509. The read buffer 509 may be a tristate buffer that is enabled by the control logic circuitry 502 during read operations. In	Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify how a person of ordinary skill in the art would understand the term in the context of the '339 patent, and that the '339 patent provides detailed description on the

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	the second side to the first side during the first time period, and to enable the data paths for a second time period subsequent to the first time period to actively drive a respective section of the second N-bit wide data associated with the second memory operation from the second side to the first side during the second time period"		another embodiment, the multiplexer 508 and the read buffer 509 may be combined in one component. In yet another embodiment, the multiplexer 508 and the read buffer 509 operations may be split over two tristate buffers, one to enable the value from Y1 to the data line 518 and another to enable the value from Y2 to the data line 518."). 17:45-52 ("Operation of a memory module using the data transmission circuit 416 may be further understood with reference to FIG. 6, an illustrative timing diagram of signals of the memory module 402. The timing diagram includes first through eighth time periods 601-608. When the memory devices 404 are synchronous memories, each of the time periods 601-608 may correspond to one clock cycle of the memory devices 404."). 18:25-65 ("The fifth, sixth, seventh, and eighth time periods 605-608 illustrate read operations with data passing to the memory controller 420 from the memory module 402. The timing diagram shows a read operation from the first group of memory devices 412A, 412C connected to the first terminals Y1 of the data transmission circuits 416 and a read operation from the second group of memory devices 412B, 412D connected to the second terminals	transmission circuit/buffer, the logic within the transmission circuit and how the logic controls and enables the data paths (including corresponding tristate buffers) for read operations. In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement. For example, Dr. Mangione-Smith may opine why it is improper to import a "fork-in-the-road" requirement into the term.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			Y2 of the data transmission circuits 416. Recalling the CAS latency described above, each read operation extends over two time periods in a pipelined manner. [¶] The read from the first group of memory devices 412A, 412C appears in the fifth time period 605 when system address and control signals 440 pass from the memory controller 420 to the control circuit 430. The control circuit 430 evaluates the address and control signals 440 to determine that data is to be read from memory devices 412A, 412C in the first group. During the sixth time period 606, the control circuit 430 supplies control signals to the control logic circuitry 502 to cause the multiplexer 58 to select data from the first terminal Y1, to enable the read buffer 509, and to disable the first tristate buffer 504 and the second tristate buffer 506. Thus, during the sixth time period 606, data bits pass from the memory devices 412A, 412C via the first terminal Y1 to data lines 518 and on to the memory controller 420. [¶] The read from the second group of memory devices 412B, 412D appears in the seventh time period 607 when system address and control signals 440 pass from the memory controller 420 to the control circuit 430. The control circuit 430 evaluates the address and control signals 440 to determine that data is to be read from memory devices 412B, 412D in the second group. During the	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			eighth time period 608, the control circuit 430 supplies control signals to the control logic circuitry 502 to cause the multiplexer 508 to select data from the second terminal Y2, to enable the read buffer 509, and to disable the first tristate buffer 504 and the second tristate buffer 506. Thus, during the eighth time period 606, data bits pass from the memory devices 412B, 412D via the second terminal Y2 to data lines 518 and on to the memory controller 420."); Figs. 5-6.	
27	"each respective n-bit-wide data buffer includes … a first set of tristate buffers configurable to drive the respective n-bit section of the write data to the respective module data lines, … a second set of tristate buffers configurable to drive the respective n-bit	No construction required (plain and ordinary meaning to a person of ordinary skill in the art in light of the specification); not indefinite; not subject to 35 U.S.C. § 112, ¶ 6.	*See* citations for the above terms.	Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify how a person of ordinary skill in the art would understand the terms in the context of the '339 patent, and that the '339 patent provides detailed description on the transmission circuit/buffer, the logic within the transmission circuit and how

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	section of the read data to the respective set of data signal lines, and logic configurable to control at least the first set of tristate buffers and the second set of tristate buffers"			the logic controls and enables the data paths (including corresponding tristate buffers) for read and write operations. In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement. For example, Dr. Mangione-Smith may opine why it is improper to import a "fork-in-the-road" requirement into the term.
1	"a module controller . . . configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write	No construction required (plain and ordinary meaning to a person of ordinary skill in the art in light of the specification); not indefinite; not subject to 35 U.S.C. § 112, ¶ 6.	*See* disclosures related to "control circuit" 430/430'. 10:17-32 ("In certain embodiments, at least one memory module 402, 402' comprises a control circuit 430, 430' configured to be operatively coupled to the system memory controller 420, 420' and to the memory devices 412, 412' of the memory module 402, 402' (e.g., via lines 442, 442'). In certain embodiments, the control circuit 430, 430' may include one or more functional devices, such as a programmable-logic device (PLD), an application specific	Dictionary definition of "controller" Comprehensive Dictionary of Electrical Engineering (2nd Ed., 2005), at 148 ("(1) the entity that enforces the desired behavior-as specified by the control objectives - of the controlled process by adjusting the manipulated inputs. The values of these inputs are either

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	data from the memory controller into a first N- bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in		integrated circuit 25 (ASIC), a field-programmable gate array (FPGA), a custom designed semiconductor device, or a complex programmable-logic device (CPLD). In certain embodiments, the control circuit 430, 430' may comprise one or more custom devices. In certain embodiments, the control circuit 430, 430' may comprise various discrete electrical elements; while in other embodiments, the control circuit 430, 430' may comprise one or more integrated circuits."); 10:33-53 ("The control circuit 430, 430' of certain embodiments is configurable to be operatively coupled to control lines 440, 440' to receive control signals (e.g., bank address signals, row address signals, column address signals, address strobe signals, and rank-address or chip-select signals) from the system memory controller 420,420'. The control circuit 430, 430' of certain embodiments registers signals from the control lines 440, 440' in a manner functionally comparable to the address register of a conventional RDIMM. The registered control lines 440, 440' are also operatively coupled to the memory devices 412, 412'. Additionally, the control circuit 430, 430' supplies control signals for the data transmission circuits 416, 416' (e.g., via lines 432, 432'), as described more fully below. The	predetermined or decided upon (computed) using on-line, i.e., real time, decision mechanism of the controller - based on the currently available information. See also controlled variable. . . . (3) a unit that directs the operation of a subsystem within a computer. For instance, a disk controller interprets data access commands from host computer (via a bus), and sends read/write, track seeking, and· other control signals to the drive. During this time, the computer can perform other tasks, until the controller signals DATA READY for transfer via the CPU bus."). Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	response to at least some of the input address and control signals"		control signals indicate, for example, the direction of data flow, that is, to or from the memory devices 412,412'. The control circuit 430,430' may produce additional chip-select signals or output enable signals based on address decoding. Examples of circuits which can serve as the control circuit 430, 430' are described in more detail by U.S. Pat. Nos. 7,289,386 and 7,532,537, each of which is incorporated in its entirety by reference herein."); *see also id.*, 1:52-56. 13:36-53 ("For example, as schematically illustrated by FIG. 4A (which corresponds generally to FIG. 3A), the data transmission circuit 416 can be operatively coupled to a single memory device 412 per rank, and both the data transmission circuit 416 and the memory device 412 per rank to which the data transmission circuit 416 is operatively coupled can each have the same bit width (e.g., 4 bits, 8 bits, or 16 bits). The data transmission circuit 416 of FIG. 4A has a bit width of 8 bits, and receives data bits 0-7 from the system memory controller 420 and selectively transmits the data bits 0-7 to selected memory devices 412A, 412B, 412C, 412D in response to the module control signals from the control circuit 430. Similarly, data transmission circuits 416' of certain embodiments can function as byte-wise	The expert will testify how a person of ordinary skill in the art would understand "module controller" in the context of the '339 patent, and that the '339 patent provides exemplary disclosures on the structure and functions of the "module controller" when it discloses and describes control circuit 430 and '430'. The expert will further testify, if needed how the address register of a conventional RDIMM at the time of the invention registers signals. In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement. For example, Dr. Mangione-Smith may opine why it is improper to import a "rank multiplication" requirement into the term. *See also* JEDEC No. 21C

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			buffer for associated memory devices 412'A, 412'B, 412'C, 412'D to which the data transmission circuits 416' are operatively coupled in response to the module control signals from the control circuit 430'"); 17:45-18:35, 18:36-65; Figures 3A-3D, 4A-4B, 5-6. 17:14-44 ("Referring again to FIG. 3A, when the memory controller 420 executes read or write operations, each specific operation is targeted to a specific one of the ranks A, B, C, and D of a specific memory module 402. The data transmission circuit 416 on the specifically targeted one of the memory modules 402 functions as a bidirectional repeater/multiplexor, such that it drives the data signal when connecting from the system memory controller 420 to the memory devices 412. The other data transmission circuits 416 on the remaining memory modules 402 are disabled for the specific operation. For example, the data signal entering on data line 518 entering into data transmission circuit 416 is driven to memory devices 412A and 412C or 412B and 412C depending on which memory devices are active and enabled. The data transmission circuit 416 then multiplexes the signal from the memory devices 412A, 412B,	DDR3 RDIMM Design Specification (Dec. 2012). [redacted] PC2100 and PC1600 DDR SDRAM RDIMM Design Specification (Jan. 2002) (IPR2022-00615, EX1032).

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			412C, 412D to the system memory controller 420. The data transmission circuits 416 may each control, for example, a nibble-wide data path or a bytewide-data path. As discussed above, the data transmission circuits 416 associated with each module 402 are operable to merge data read signals and to drive data write signals, enabling the proper data paths between the system memory controller 420 and the targeted or selected memory devices 412. Thus, the memory controller 420, when there are four four-rank memory modules, sees four load-reducing switching circuit loads, instead of sixteen memory device loads. The reduced load on the memory controller 420 enhances the performance and reduces the power requirements of the memory system, as compared with, for example, the conventional systems described above with reference to FIGS. 1A, 1B and 2A-2D.”). U.S. 7,289,386, 12:13-26:19 (control structure and function, including signaling and control in back-to-back read operations); *see also generally* (describing C/A signals for read/write operations and the resulting operation), 6:63-7:29.	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			U.S. 7,532,537 (see descriptions related to control circuit 40 and register 220). 4:16-47 ("One method for increasing memory space is based on an address decoding scheme. This method is very widely adopted in the electronics industry in designing Application-Specific Integrated Circuit (ASIC) and System-On-Chip (SOC) devices to expand system memories. Another method increases the addressable memory space without extensive alteration of the software or hardware of an existing electronics system. This method combines chip-select signals with an address signal to increase the number of physically addressable memory spaces (e.g., by a factor of 2, by a factor of 4, by a factor of 8, or by other factors as well). [¶] These methods have several shortcomings. For example, since these methods increase the addressable memory space by directly adding memory chips, a heavier load is presented to the outputs of the system controller and the outputs of the memory devices, resulting in a slower system. Also, increasing the number of memory devices results in higher power dissipation. In addition, since an increase in the number of memory devices on each memory module alters the physical properties of the memory module while the system board remains the same, the	

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			overall signal (transmission line) wave characteristics deviate from the original design intent or specification. Furthermore, especially when registered DIMMs (RDIMMs) are used, the increase in the number of the memory devices translates to an increase in the distributed RC load on the data paths, but not on the control paths (e.g., address paths), thereby introducing uneven signal propagation delay between the data signal paths and control signal paths. As used herein, the terms "control lines" and "control paths" include address lines or paths and command lines or paths, and the term "control signals" includes address signals and command signals."	
11	"a module controller . . . configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write	No construction required (plain and ordinary meaning to a person of ordinary skill in the art in light of the specification); not indefinite; not subject to 35 U.S.C. § 112, ¶ 6.	*See* above.	*See* above.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	data from the memory controller into a first N- bit-wide rank among the multiple N-bit-wide ranks, and to output registered address and control signals in response to the input address and control signal, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to transmit module control signals to the n/2 data			

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	transmission circuits in response to the input address and control signals"			
19	"a module controller . . . configurable to receive from the memory controller via the address and control signal lines first address and control signals for a first memory operation to read first N-bit-wide data from a first N-bit-wide rank among the multiple ranks and to subsequently receive second address and control signals for	No construction required (plain and ordinary meaning to a person of ordinary skill in the art in light of the specification); not indefinite; not subject to 35 U.S.C. § 112, ¶ 6.	*See* above.	*See* above. Expert testimony on the understanding by a person of ordinary skill in the art of the term at the time of the inventions in light of the intrinsic evidence and knowledge of the person. The expert will testify how a person of ordinary skill in the art would understand "module controller" in the context of the '339 patent, and that the '339 patent provides exemplary disclosures on the structure and functions of the "module controller" when it discloses and describes control circuit 430 and '430'. The expert will further testify, if needed how the address register of a

Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	a second memory operation to read second N-bit-wide data from a second N-bit-wide rank among the multiple ranks, the module controller being further configurable to output first registered address and control signals for the first memory operation in response to receiving the first address and control signals and to output second registered address and control signals for the second memory			conventional RDIMM at the time of the invention registers signals. In addition, if the expert disagrees with any of Samsung's proposed constructions, he will also provide testimony to explain the reasons for his disagreement. For example, Dr. Mangione-Smith may opine why it is improper to import a "rank multiplication" requirement into the term. *See also* JEDEC No. 21C DDR3 RDIMM Design Specification (Dec. 2012). [redacted] PC2100 and PC1600 DDR

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	operation in response to receiving the second address and control signals, wherein the first registered address and control signals cause the first N-bit-wide rank to output the first N-bit-wide data associated with the first memory operation, and the second registered address and control signals cause the second N-bit-wide rank to output the second N- bit-wide data associated with the second memory operation, wherein the module controller			SDRAM RDIMM Design Specification (Jan. 2002) (IPR2022-00615, EX1032).

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	is further configurable to output first module control signals for the first memory operation in response to receiving the first address and control signals and to output second module control signals for the second memory operation in response to receiving the second address and control signals"			
27	"a module controller . . . configurable to receive from the memory controller via the address and	No construction required (plain and ordinary meaning to a person of ordinary skill in the art in light of the specification); not indefinite; not	*See* above.	*See* above.

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	control signal lines first address and control signals for a memory write operation and to subsequently receive second address and control signals for a memory read operation, the module controller being further configurable to output first registered address and control signals and first module control signals for the memory write operation in response to the first address and control signals, and to output second registered address and	subject to 35 U.S.C. § 112, ¶ 6		

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Claim(s)	Term	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
	control signals and second module control signals for the memory read operation in response to the second address and control signals"			

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CERTIFICATE OF SERVICE

I hereby certify that, on August 23, 2022, a copy of the foregoing Exhibit A was served to all counsel of record.

/s/ Jason Sheasby
Jason Sheasby